ARTICLE

Fully Transparent Pixel Circuits Driven by Random Network Carbon Nanotube Transistor Circuitry

Sunkook Kim,[†,‡] Seongmin Kim,[†] Jongsun Park,[§] Sanghyun Ju,[⊥] and Saeed Mohammadi[†,*]

[†]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, [‡]Samsung Advanced Institute of Technology, San #14-1 Nongseo-do, Giheung-gu, Yongin-si, Gyeonggi-do, Korea 446-712, [§]School of Electrical and Computer Engineering, Korea University, Anam-dong, Seongbuk-Gu, Seoul 131-701, Republic of Korea, and [⊥]Department of Physics, Kyonggi University, Suwon, Kyonggi-Do 443-760, Republic of Korea

ABSTRACT Optically transparent and mechanically flexible thin-film transistors have recently attracted attention for next generation transparent display technologies. Driving and switching transistors for transparent displays have challenging requirements such as high optical transparency, large-scale integration, suitable drive current (I_{on}) in the microampere range, high on/off current ratio (I_{on}/I_{off}), high field-effect mobility, and uniform threshold voltage (V_{th}). In this study, we demonstrate fully transparent high-performance and high-yield thin-film transistors based on random growth of a single-walled carbon nanotube (SWNT) network that are easy to fabricate. High-performance SWNT-TFTs exhibit optical transmission of 80% in visible wavelength, I_{on}/I_{off} higher than 10^3, and a high yield with reproducible electrical characteristics.

KEYWORDS: carbon nanotube · transparent · thin-film transistor · network nanotube · driving circuit · pixel · OLED

Future nanoelectronics require technologies with light-weight, transparent, and flexible characteristics for applications such as conformal integration, heads-up displays, and printable/lightweight displays that are embedded within plastic shells of equipment or textile. Advances in materials and processing strategies for nanoelectronic devices including the use of semiconductor nanowires (NWs), single-walled carbon nanotubes (SWNTs), and low-leakage high-K gate dielectrics offer unique functionalities in nanocircuits/displays and active-matrix electronics such as low operating voltages, optical transparency, mechanical flexibility, and high performance including high mobilities in comparison with poly/amorphous Si thin-film transistors (TFTs) or organic TFTs. In this context, transistors incorporating semiconducting SWNTs and NWs are of particular interest for future display devices.[1−3] There are several challenges to surmount before such devices can be utilized in commercial products. Many of the reported NW and SWNT device[3−8] fabrication approaches are not well-suited for commercial electronics, due to their non-uniformity, low reliability characteristics, and processing challenges.

Key challenges to manufacture commercial high-performance nanoelectronic products that are robust, transparent, and flexible are integration of SWNT or NW materials with improved and stable transistor characteristics, suitable on current (I_{on} ~ μA) to derive high-resolution organic light-emitting diode (OLED) pixels, high on/off current ratio (I_{on}/I_{off}), high field-effect mobility (μ_{eff}), steep subthreshold slope (S), and uniform threshold voltage (V_{th}). It is also important to achieve low voltage operation, uniform performance, and high reliability for such flexible and transparent devices. Such a technology should yield the ability to integrate individual nano-based transistors into a scalable pixel driver circuit on a large-area substrate. Random network SWNTs and horizontally synthesized aligned SWNTs as an active channel are two candidate approaches for these aforementioned characteristics. Here, a statistical average of multipath transport can provide device uniformity regardless of individual transport characteristics of SWNTs in the array.

In this paper, we demonstrate fully transparent display devices based on integrating random network SWNT-TFTs and drive/switch display pixels. The building and positioning of uniformly assembled SWNT transistor arrays on large quartz substrates and specific patterning to control the current level of the device are studied. Device yield and device-to-device performance variations are also investigated. SWNT device performance enhancement in terms of I_{on}/I_{off}, V_{th}, μ_{eff}, and S using several post-treatments is also investigated. Optimized random network SWNT-TFTs are used as the demonstration of transparent nanodisplay

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*Address correspondence to saeedm@purdue.edu.

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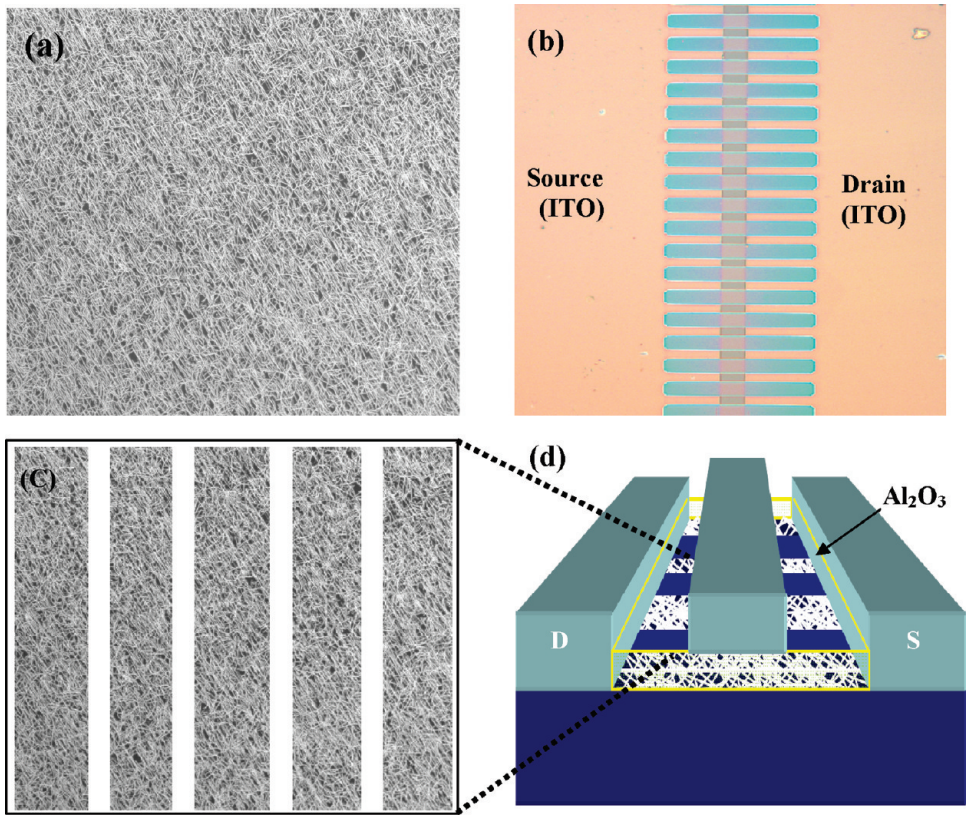

Figure 1. Synthesis of random network SWNTs and transparent SWNT-TFT fabrication. High-density random network CNTs: scanning electron microscope (SEM) image of randomly grown SWNT network on quartz wafer using 2−3 Å thick e-beam-evaporated Fe as catalyst. (b) PR stripe on network CNTs: the optical image of photoresist (PR) patterns for selectively etching of SWNTs using oxygen plasma etcher. (c) CNT stripes after O_2 plasma etcher: the magnified view of network stripes of the SWNT network in the channel region of a TFT device. The nanotubes in the white region are removed by etching. (d) Schematic view of a top-gated SWNT network TFT with a 30 nm thick ALD Al_2O_3 gate dielectric.

elements for driving and switching transistors in an active matrix panel.

Figure 1 shows a cross-sectional view and fabrication of a transparent SWNT-TFT for an active-matrix organic light-emitting diode (AMOLED) with a channel that consists of random network SWNTs grown using an Fe catalytic chemical vapor deposition (CVD) method on a quartz substrate. A 30 nm thick Al_2O_3 layer is grown on top of the SWNT film using an atomic layer deposition system with alternating pulses of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) at 300 °C in a carrier N_2 gas.[6] The ALD-deposited Al_2O_3 layer isolates SWNT-TFTs from their environment while facilitating stable DC characteristics. After drain source patterns are defined, transparent ITO source−drain electrodes (100 nm) are deposited using the ion-assisted deposition (IAD) method at room temperature. Post-deposition annealing is performed to improve the subthreshold slope in Ar at ambient conditions of 350 °C for 10 min.[2]

Figure 1a shows a scanning electron micrograph of a randomly grown SWNT network on a quartz wafer. An evaporated 2−4 Å Fe catalyst film using an Airco e-beam evaporator is synthesized to grow carbon nanotubes, enabling the growth of a uniform network of SWNTs on a large quartz substrate. The conventional catalyst of ferritin (Sigma, diluted 20 times in deionized water)[1,4,5] is a solution-based distribution used to grow a random network of carbon nanotubes, on which it is impossible to grow a uniform film on a whole wafer. Instead, a uniformly evaporated Fe catalyst is used to synthesize a uniform density of SWNTs on a 3 in. wafer. On the basis of the percolation theory,[9−11] stripes of network SWNTs are etched with channel stripe widths (W_{stripe}) of 5 μm and spacings of 2 μm in order to increase the I_{on}/I_{off} without performing a post-process electrical burning, as shown in Figure 1c. The etching of the SWNT network is performed by exposure of patterned regions of the film (patterned by Shipley 1805 photoresist) to an oxygen plasma (at 2 mTorr Ar and 4 mTorr O_2 for 3 min). Random network of CNTs with diameters of 1−3 nm and stick lengths (L_{stick}) of 3−5 μm and specific densities of semiconducting CNTs (D_S) and metallic tubes (D_M) are distributed along the channel region to form a percolating path from source to drain for SWNT-TFTs with various strip lengths (L_C). On the basis of the percolation theory, high $I_{on/off}$ ratio is achieved as long as the percolation threshold (D_P) is smaller than D_S and larger than D_M since all percolation paths involve at least one semiconducting tube stick. In our study, the total tube density (D_M and D_S) of 5−7 μm^{-2} can be uniformly achieved on a quartz substrate, which is higher than the percolation threshold density of $D_P \sim$

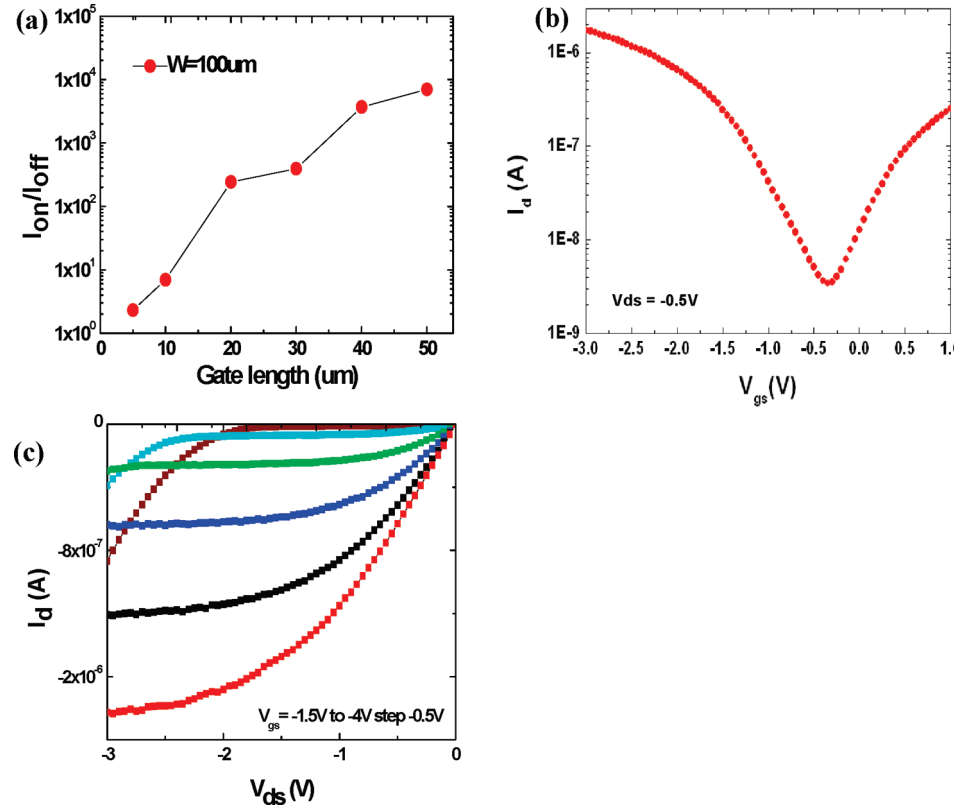

Figure 2. Electrical characteristics of thin-film transistors based on SWNT network stripes with transparent ITO source/drain/gate electrodes. (a) Ratio of I_{on}/I_{off} scaling *versus* channel length with the same device geometry. Measured characteristics of p-type SWCNT-TFTs with a gate length of 40 μm and a source/drain width of 100 μm. (b) I_d-V_{gs} characteristics of fully transparent SWNT-TFTs at $V_{ds}= -0.5$ V *versus* gate source voltage. Generally, ALD alumina encapsulation results in the change from p-type semiconducting nanotube to ambipolar. The phenomenon is attributed to a change in the Schottky barriers at the CNT−metal contacts caused by oxygen desorption during annealing. (c) I_d-V_{ds} characteristics of fully transparent SWNT-TFTs. V_{GS} ranges from −1.5 to −4 V in −0.5 V steps.

$1/L_{stick}^2 \sim 0.04-0.11$ μm^{-2}.[10−13] Strip width is set to 5 μm, which is similar to the length of SWNT to improve the $I_{on/off}$ ratio for TFTs. $W_{stripe}/L_{stick} \sim 1.0-1.66$ is achieved, where reduction in a fraction of tubes near the stripe can be translated into an overall reduction in "average" tube length $\langle L_{stick,eff}\rangle$ in the channel and, therefore, percolation threshold being pushed to the D_M to D_S interval to ensure high $I_{on/off}$ ratio. In such W_{stripe}/L_{stick}, the probability of a metallic subnetwork being directly bridged to the contacts is reduced to achieve a high I_{on}/I_{off} ratio. A high I_{on}/I_{off} ratio above 10^3 is observed for strip lengths L_C higher than 40 μm (*i.e.*, $L_C/W_{stripe} > 8$), where the probability of a metallic subnetwork in gate length of 40 μm is a rare event, due to the fact that all metallic sticks cannot directly bridge source and drain.

Major drawbacks of transparent and portable displays based on α-Si and poly-Si TFTs are low optical transmittance levels and poor flexibility. Additionally, transistors built in these two technologies consume a considerable amount of power, which adversely affects their application in portable displays. Recent publications, however, suggest that an attractive candidate for a transparent circuit to overcome these limitations would be single-walled nanotubes,[4,5] graphene,[14,15] and nanowire transistors,[3] which have high mobilities (10−1500 cm^2 V^{-1} s^{-1}) and high transparency (>80%) in visible wavelengths. These studies mainly contributed to improve single transistor performance rather than an integrated circuit optimization for active-matrix organic light-emitting diode thin-film transistor (AMOLED-TFT) panels. In this study, we deviate from single transistor optimization to large-scale integration of devices to derive OLED pixels. As shown in Figure 1b, SWNT-TFTs with different stripe width W and channel length L_C are designed to determine the effect of stripe geometry on the on current and I_{on}/I_{off} ratio. As shown in Figure 2a, it is observed that channel lengths higher than 40 μm, which corresponds to $L_C/W_{stripe} > 8$, reliably result in I_{on}/I_{off} ratio higher than 10^3. The drop in I_{on}/I_{off} ratio for smaller channel lengths is due to a higher percentage of metallic tube pathways that reside within the gate length (L_C). Measured current−voltage ($I-V$) characteristics for a representative SWNT-TFTs (gate length of 40 μm and an overall width of 100 μm) are shown in Figure 2b,c. The device achieves a maximum on current of −2.5 μA, a transconductance of 0.2 μS, and an I_{on}/I_{off} ratio >10^3. The field-effect mobility (μ_{eff}) is computed from the transconductance, defined by $g_m = [\partial I_d/\partial V_{gs}]_{V_{ds}=constant}$. On the basis of the standard mod-

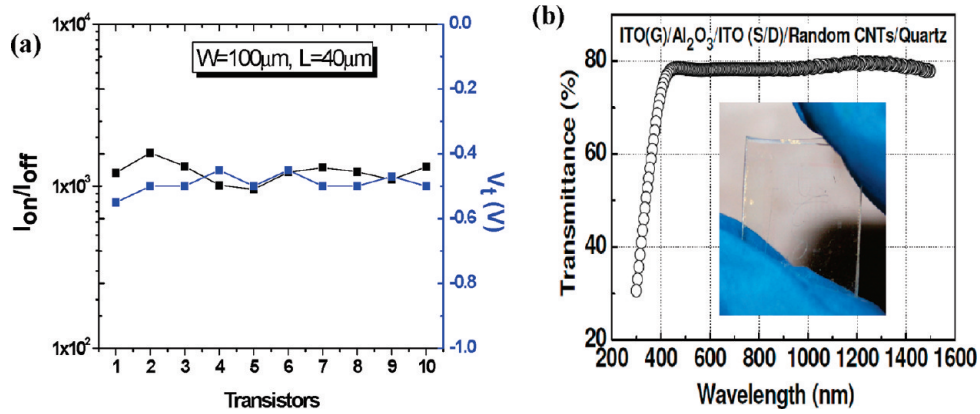

Figure 3. (a) I_{on}/I_{off} ratio and threshold voltage (V_{th}) of 10 representative TFTs. More than 92% of SWNT-TFTs achieve identical electrical properties. (b) Optical transmission spectrum of a 1.5 × 1.5 cm quartz substrate after processing of SWNT-TFTs is complete.

els of metal−oxide−semiconductor field-effect transistors and the measured current−voltage characteristics, the field-effect mobility ($\mu_{eff} = Lg_m/(WC_{ox}V_{ds})$) is calculated as 16−22 $cm^2\ V^{-1}\ s^{-1}$ for the representative SWNT network TFT with ITO electrodes. The subthreshold swing ($S = dV_{gs}/[d(\log_{10}I_d)]$) is about 400−500 mV per decade.

Figure 3a shows the measured threshold voltage, V_{th} (blue), and I_{on}/I_{off} (black) values of 10 representative SWNT-TFTs of W/L = 100 μm/40 μm, showing the average values of I_{on}/I_{off} ratio of 1 × 10^3 and V_{th} of −0.5 V. More than 90% of SWNT-TFTs achieve uniform device performance with rapid switching and electrical performance. Figure 3b shows the optical transmission spec-

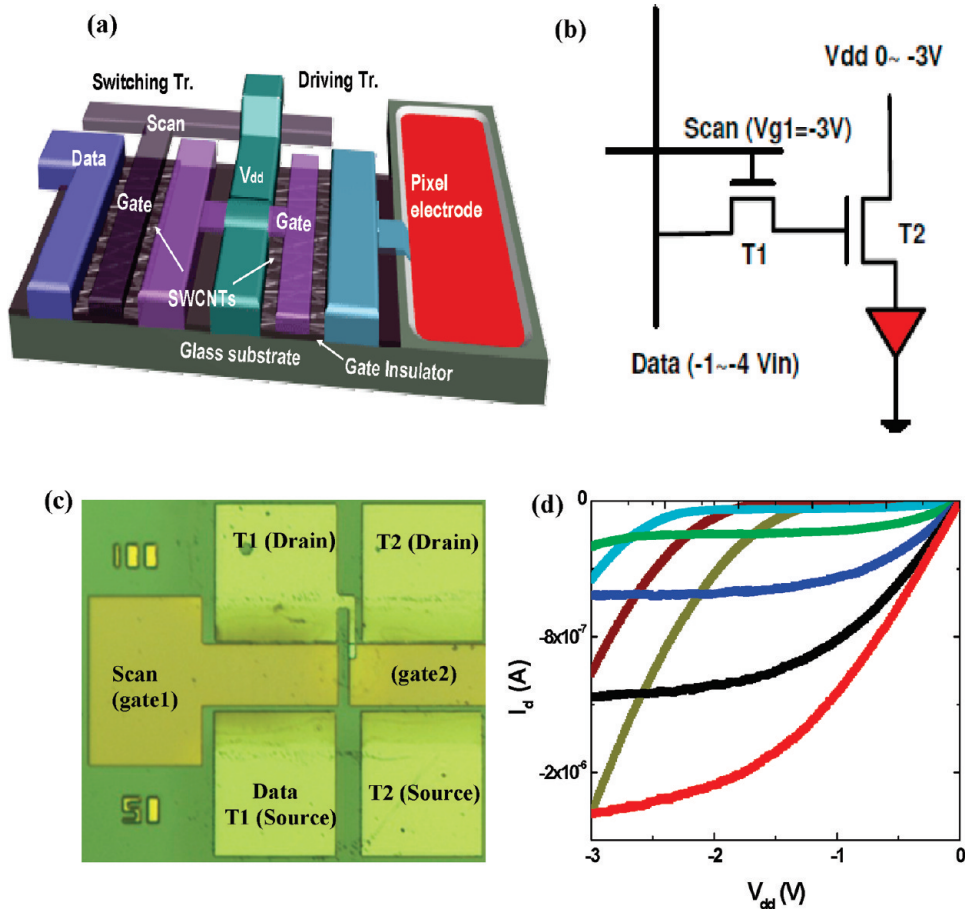

Figure 4. (a) Cross-sectional diagram of a prototype transparent active-matrix driving circuit composed of 1 driving SWNT Tr (D.Tr) and 1 switching SWNT Tr (S.Tr) for a transparent organic light-emitting diode. (b) Schematic diagram for the circuit of a single pixel. (c) Optical image of a fabricated SWNT-TFT composed of 1 driving SWNT Tr and 1 switching SWNT Tr. (d) Output current−voltage characteristics for a single-pixel circuit consisting of one switching transistor and one driving transistor.

trum with a transparency of greater than 80% in the 350−1500 nm wavelength range through a 1.5 cm ×1.5 cm quartz substrate with TFT devices. The inset in Figure 3b shows an optical image of random network SWNT-TFTs. Therefore, significant progress toward commercialization of transparent TFT based on random network SWNTs with high optical transparency of ~80%, high field-effect mobility of 16−22 $cm^2 V^{-1} s^{-1}$, large-scaled integration, and improved uniformity for device-to-device variation regardless of individual transport SWNTs forming in the network has been achieved.

Figure 4a shows a prototype of a transparent AMOLED display driven by network SWNT-TFTs. The proposed SWNT-TFT array can drive and switch a unit pixel composed of OLED-sustaining constant cell gap, where the transparent characteristics of SWNT-TFTs allows the design of vertical structure with a high aperture ratio. The equivalent pixel circuit is shown in Figure 4b. In the driver circuit, the OLED is controlled with one switching transistor (T1) and a driver transistor (T2) at each pixel. When the scan line is driven, the switching transistor is switched on and the signal from the data line is supplied to the driver transistor to drive the OLED. The pixel circuits assembled by these p-type semiconducting SWNT-TFTs are operated with several steps of the data line voltage (drain of T1: −1.0 to −4.0 V in 0.5 V steps). The steps in the data line voltage correspond to changes in V_{gs} for the driver transistor (T2). The transistor circuit exhibits ~2.5 μA at $V_{dd} = -2.0$ V, $V_{scan} = -3.0$ V, and $V_{data} = -4.0$ V.

In summary, fully transparent pixel circuits using random network SWNT-TFTs are demonstrated, exhibiting significant improvement in transistor characteristics. The devices show high device yield of more than 90% and an optical transmittance of more than 80%. It is expected that power consumption can be dramatically decreased by enhancing the maximum aperture ratio due to a significant optical transparency and low operating voltage in transistor arrays on pixels. These results indicate that SWNT-TFTs are promising for active driver and addressing circuits for applications in future flexible and/or transparent display devices.

METHODS

Synthesis of Random Network SWNTs and Its Stripe. Quartz substrate is cleaned by a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), used to remove organic residues off substrate. Transparent ITO reference marks are deposited by ion-assisted deposition (IAD) for post-litho process. Then, 2−5 Å thick catalysts are deposited by electron beam deposition of iron (3×10^{-6} Torr; Temsescal CV-8) overall wafer. A flow of methane (CH_4) at 150 sccm and hydrogen (H_2) at 50 sccm at 900 °C for 15 min yields random network SWNTs on a quartz substrate, as shown in Figure 1a. During the growth of CNTs, quartz wafers are subjected to high temperatures and a subsequent rapid ramp-down of the temperature in the growth chamber, which may cause the quartz wafer to break. To mitigate this problem, the quartz wafer is placed on a Si wafer to prevent a rapid change in the temperature. Experimentally, at hinner catalyst can support the growth of more dense SWNTs. UV photolithography (Shipley 1813) is used to protect 5 μm wide individual SWNT network stripes. The unprotected SWNTs are etched away with oxygen reactive ion etching (RIE). The photoresist is removed by acetone and isopropyl alcohol. The remaining SWNT network stripes form the channel of thin-film transistors, where the position of the SWNT network is based on the original ITO reference mark.

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REFERENCES AND NOTES

1. Cao, Q.; Kim, H.; Pimparkar, N.; Kulkarni, J. P.; Wang, C.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates. *Nature* **2008**, *454*, 495–500.
2. Kim, S.; Ju, S.; Back, J. H.; Xuan, Y.; Ye, P. D.; Shim, M.; Janes, D. B.; Mohammadi, S. Fully Transparent Thin-Film Transistors Based on Aligned Carbon Nanotube Arrays and Indium Tin Oxide Electrodes. *Adv. Mater.* **2009**, *21*, 564–568.
3. Ju, S.; Facchetti, A.; Xuan, Y.; Liu, J.; Ishikawa, F.; Ye, P.; Zhou, C.; Marks, T. J.; Janes, D. B. Fabrication of Fully Transparent Nanowire Transistors for Transparent and Flexible Electronics. *Nat. Nanotechnol.* **2007**, *2*, 378–384.
4. Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. Self-Aligned Ballistic Molecular Transistors and Electrically Parallel Nanotube Arrays. *Nano Lett.* **2004**, *4*, 1319–1322.
5. Cao, Q.; Hur, S.-H.; Zhu, Z.-T.; Sun, Y.; Wang, C.; Meitl, M. A.; Shim, M.; Rogers, J. A. Highly Bendable, Transparent Thin-Film Transistors That Use Carbon-Nanotube-Based Conductors and Semiconductors with Elastomeric Dielectrics. *Adv. Mater.* **2006**, *18*, 304–309.
6. Kim, S.; Xuan, Y.; Back, J. H.; Ye, P. D.; Shim, M.; Mohammadi, S. Atomic Layer Deposited Al_2O_3 for Gate Dielectric and Passivation Layer of Single-Walled Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2007**, *90*, 163108.
7. Tans, S. J.; Verschueren, R. M.; Dekker, C. Room-Temperature Transistor Based on A Single Carbon Nanotube. *Nature* **1998**, *393*, 49–52.
8. Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2003**, *3*, 193–198.
9. Pimparkar, N.; Cao, Q.; Rogers, J. A.; Alam, M. A. Theory and Practice of Nanonet Thin Film Transistors. *Nano Res.* **2009**, *2*, 167–175.
10. Pimparkar, N.; Kumar, S.; Cao, Q.; Rogers, J. A.; Murthy, J. Y.; Alam, M. A. Limits of Performance Gain of Aligned CNT over Randomized Network: Theoretical Predictions and Experimental Validation. *IEEE Electron Device Lett.* **2007**, *28*, 593–595.
11. Kirkpatrick, S. Percolation and Conduction. *Rev. Mod. Phys.* **1973**, 574–588.
12. Dobson, M. A.; Garland, J. C. Violation of Sum Rules by Random Phase Approximation Surface Response Calculations Based on a Density-Functional Ground-State Description. *Phys. Rev. B* **1985**, *32*, 6255–6260.
13. Frank, D. J.; Lobb, C. J. Highly Efficient Algorithm for Percolative Transport Studies in Two Dimensions. *Phys. Rev. B* **1988**, *37*, 302–307.
14. Bai, J.; Zhong, X.; Jiang, S.; Huang, Y.; Duan, X. Graphene Nanomesh. *Nat. Nanotechnol.* **2010**, *5*, 190–194.
15. Wu, J.; Agrawal, M.; Becerril, H. A.; Bao, Z.; Liu, Z.; Chen, Y.; Peumans, P. Organic Light-Emitting Diodes on Solution-Processed Graphene Transparent Electrodes. *ACS Nano* **2010**, *4*, 43–48.